CONFIGURING FPGAs AND THE LIKE USING ONE OR MORE SERIAL MEMORY DEVICES

ABSTRACT

The configuration architecture for a programmable device, such as an FPGA, includes one or more memory devices connected directly to the FPGA such that the FPGA can be configured with configuration data stored in the memory devices without transmitting the configuration data via a controller connected between any of the memory devices and the FPGA. In one embodiment, the FPGA has an Serial Peripheral Interface (SPI) that is connected to the SPI interface of each of one or more SPI serial flash PROMs operating as boot PROMs. When there are two or more boot PROMs, each PROM stores a portion of the FPGA's configuration data and the FPGA interleaves the data from multiple boot PROMs to generate a serial configuration data bitstream. The present invention enables boot PROMs having different sizes and/or storing different amounts of configuration data to be simultaneously connected to an FPGA to support efficient configuration architectures.